WHAT IS CLAIMED IS:

1. A method of programming a PMOS stacked gate memory cell that includes spaced apart p-type diffusion regions formed in an n-type semiconductor substrate to define a substrate channel region therebetween, a conductive floating gate electrode formed over the channel region and separated therefrom by gate dielectric material, and a conductive control gate electrode formed over the floating gate electrode and separated therefrom by integrate dielectric material, the method comprising:

a. applying a negative voltage to the drain region of the PMOS memory cell;

b. applying a potential to the control gate electrode of the PMOS memory cell such that electrons are attracted to the floating gate electrode through the gate dielectric material;

c. establishing a correlation between floating gate electron injection current and substrate current;

d. monitoring substrate current;

e. providing a feedback correction to the control gate potential such that the substrate current is maintained at a maximum.